WHAT IS CLAIMED IS:

1. A discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal.

2. The discrete time analog filter according to claim 1, further comprising means for direct sampling, wherein the cascade of single pole IIR filters and means for direct sampling together implement a high order filter devoid of amplifiers

3. The discrete time analog filter according to claim 2, wherein the means for direct sampling comprises a multi-tap direct sampling mixer

4. The discrete time analog filter according to claim 1, further comprising means for direct sampling, and at least one amplifier stage, wherein the cascade of single pole IIR filters, the means for direct sampling, and the at least one amplifier stage together implement a high order filter.

5. The discrete time analog filter according to claim 4, wherein the means for direct sampling comprises a multi-tap direct sampling mixer.

6. The discrete time analog filter according to claim 1, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers

7. The discrete time analog filter according to claim 1, wherein the cascade of single pole IIR filters is operational to create a uni-directional flow of information, signal, or charge and disallow any feedback from a later filter stage to an earlier filter stage.

8. The discrete time analog filter according to claim 1, wherein the cascade of single pole IIR filters comprises a history capacitor that is charged together with a first rotating capacitor in a first capacitor bank for a predetermined time period while a charge in a second capacitor bank is charge shared with a buffer capacitor and a second rotating capacitor, and wherein during a subsequent time period, the first capacitor bank holding its charge is charge shared with the buffer capacitor while the second capacitor bank which was charge shared in a previous time period now collects new samples together with the history capacitor.

9. The discrete time analog filter according to claim 8, wherein the charge on the second rotating capacitor is reset only after it charge shares with the buffer capacitor on the following stage and before it obtains a new sample from the preceding stage.

10. The discrete time analog filter according to claim 1, further comprising:

a comparator responsive to the filter output signal to generate an output signal there from; and

a negative feedback loop enclosing the cascade of single pole IIR filters and the comparator such that the input signal consists of an RF input signal combined with a negative feedback signal flowing in the negative feedback loop.

11. The discrete analog filter according to claim 10, wherein the cascade of single pole IIR filters together operate as a loop filter inside a sigma delta loop.

12. The discrete analog filter according to claim 10, wherein the input signal consists of an RF input signal minus a negative feedback signal flowing in the negative feedback loop.

13. The discrete analog filter according to claim 10, wherein the comparator comprises an ADC.

14. The discrete analog filter according to claim 13, wherein the ADC comprises a multi-bit flash ADC.

15. The discrete analog filter according to claim 10, wherein the negative feedback loop comprises a digital-to-analog converter (DAC).

16. The discrete time analog filter according to claim 1, wherein the single pole IIR filters are comprised solely of switches and capacitors.

17. The discrete time analog filter according to claim 1, wherein the cascade of single pole IIR filters comprises:

a history capacitor;

a first set of rotating capacitors, wherein a subset of the first set of rotating capacitors is connected to the history capacitor;

a buffer capacitor connected to a different subset of the first set of rotating capacitors; and

a second set of rotating capacitors, wherein a subset of the second set of rotating capacitors is connected to the buffer capacitor.

18. The discrete time analog filter according to claim 17, wherein after a predetermined period of time, another subset of the first set of rotating capacitors is connected to the history capacitor and another subset of the second set of rotating capacitors is connected to the buffer capacitor, such that the respective subsets of rotating capacitors connected to the history capacitor and buffer capacitor operate in a ping-pong fashion.

19. The discrete time analog filter according to claim 17, wherein each set of rotating capacitors consists of two capacitors.

20. The discrete time analog filter according to claim 17, wherein the first and second set of rotating capacitors are configured as a pair of capacitor banks that operate in a ping-pong fashion with respect to one another.

21. A receiver front-end comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal.

22. The receiver front-end according to claim 21, further comprising means for direct sampling, wherein the cascade of single pole IIR filters and means for direct sampling together implement a high order filter devoid of amplifiers

23. The receiver front-end according to claim 22, wherein the means for direct sampling comprises a multi-tap direct sampling mixer

24. The receiver front-end according to claim 21, further comprising means for direct sampling, and at least one amplifier stage, wherein the cascade of single pole IIR filters, the means for direct sampling, and the at least one amplifier stage together implement a high order filter.

25. The receiver front-end according to claim 24, wherein the means for direct sampling comprises a multi-tap direct sampling mixer.

26. The receiver front-end according to claim 21, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers

27. The receiver front-end according to claim 21, wherein the cascade of single pole IIR filters is operational to create a uni-directional flow of information, signal, or charge and disallow any feedback from a later filter stage to an earlier filter stage.

28. The receiver front-end according to claim 21, wherein the cascade of single pole IIR filters comprises a history capacitor that is charged together with a first rotating capacitor in a first capacitor bank for a predetermined time period while a charge in a second capacitor bank is charge shared with a buffer capacitor and a second rotating capacitor, and wherein during a subsequent time period, the first capacitor bank holding its charge is charge shared with the buffer capacitor while the second capacitor bank which was charge shared in a previous time period now collects new samples together with the history capacitor.

29. The receiver front-end according to claim 28, wherein the charge on the second rotating capacitor is reset only after it charge shares with the buffer capacitor on the following stage and before it obtains a new sample from the preceding stage.

30. The receiver front-end according to claim 21, further comprising:

a comparator responsive to the filter output signal to generate an output signal there from; and

a negative feedback loop enclosing the cascade of single pole IIR filters and the comparator such that the input signal consists of an RF input signal combined with a negative feedback signal flowing in the negative feedback loop.

31. The receiver front-end according to claim 30, wherein the cascade of single pole IIR filters together operate as a loop filter inside a sigma delta loop.

32. The receiver front-end according to claim 30, wherein the input signal consists of an RF input signal minus a negative feedback signal flowing in the negative feedback loop.

33. The receiver front-end according to claim 30, wherein the comparator comprises an ADC.

34. The receiver front-end according to claim 33, wherein the ADC comprises a multi-bit flash ADC.

35. The receiver front-end according to claim 30, wherein the negative feedback loop comprises a digital-to-analog converter (DAC).

36. The receiver front-end according to claim 21, wherein the single pole IIR filters are comprised solely of switches and capacitors.

37. The receiver front-end according to claim 21, wherein the cascade of single pole IIR filters comprises:

a history capacitor;

a first set of rotating capacitors, wherein a subset of the first set of rotating capacitors is connected to the history capacitor;

a buffer capacitor connected to a different subset of the first set of rotating capacitors; and

a second set of rotating capacitors, wherein a subset of the second set of rotating capacitors is connected to the buffer capacitor.

38. The receiver front-end according to claim 37, wherein after a predetermined period of time, another subset of the first set of rotating capacitors is connected to the history capacitor and another subset of the second set of rotating capacitors is connected to the buffer capacitor, such that the respective subsets of rotating capacitors connected to the history capacitor and buffer capacitor operate in a ping-pong fashion.

39. The discrete time analog filter according to claim 37, wherein each set of rotating capacitors consists of two capacitors.

40. The discrete time analog filter according to claim 37, wherein the first and second set of rotating capacitors are configured as a pair of capacitor banks that operate in a ping-pong fashion with respect to one another.